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BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/747,977 | RUDD ET AL. | |
| | Examiner | Art Unit | |
| | Reba I. Elmore | 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9,13-31,34-36,38-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-9,13-31,34-36,38-40,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

# DETAILED ACTION

1. Claims 1-9, 13-31, 34-36, 38-40 and 42-43 are presented for examination. Claims 10-12, 32-33, 37, 41 and 44-46 have been cancelled by the amendment filed June 24, 2008.

## *SPECIFICATION*

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## *35 USC § 112, 1st Paragraph*

3. The rejection of claims 1-9, 13-31, 34-36, 38-40 and 42-43 as being rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement is ***maintained*** and repeated below.

4. The following is a quotation of the first paragraph of 35 USC § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-9, 13-31, 34-36, 38-40 and 42-43 are rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. The volatile and nonvolatile language in the claims and the specification is not adequately described as being status data or ownership data. This language also appears to apply

to either cache lines or segments of lines which also adds to the confusing language. As these terms are not terms in the memory art which apply to cache ownership or cache coherency applications, the written description fails to comply with the written description requirement.

7. A means for tracking shared data is also suggested in the abstract and claim 17. This language has also been added to the new claims, however, nothing in the specification or the drawings give details as to how the tracking is accomplished or what is doing the tracking or what is meant by tracking shared data. Tracking shared data and maintaining status of cache lines or cache segments are not necessarily the same activity and without further explanation this language is not adequately defined in the written description.

8. The written description persistently uses non-descriptive, non-specific language. The law requires that the written description be clear and precise as to how the Applicant performs such activities as those claimed. The specification uses terms which are not further defined, yet, these terms are essential subject matter as they are included in the claims. If the broadest, common sense interpretation is not correct, the specification does not properly define the terms which the claims rely upon for patentability. The novelty of the present invention must be disclosed in such detail as to allow one of ordinary skill in the art to make and use the invention without undue experimentation. Such details for the actual inventive concepts have not been given in the present disclosure. Legal support for these reasons for a determination that the written disclosure is not adequate can be found in the recent US Court of Appeals for the Federal Circuit, Automotive Technologies International, Inc., v. BMS of North America, Inc … (2006-1013,-1037).

9. The rejection of claims 1-31 as failing to comply with the enablement requirement under

35 USC § 112, 1st paragraph is ***withdrawn*** due to the amendment.

## *35 USC § 112, 2nd Paragraph*

10. The rejection of claims 1-9, 13-31, 34-36, 38-40 and 42-43 under 35 USC § 112, 2nd paragraph, as being indefinite is ***withdrawn*** due to the amendment. The following rejections are given due to the amendment.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-9, 13-31, 34-36, 38-40 and 42-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. It is not clear as to what is meant by the language 'executing a first second state load request' as given in claim 13.

14. The claims are now directed to first states, second states and first status and second status, however, when relied on for explanation, the present specification makes it clear this language is still the 'volatile' and 'nonvolatile' language previously in the claims. Nothing else in t he specification is provided for the states and statuses which therefor means this language still has the same indefiniteness as before. The claim language uses the following terms 'modified volatile', 'exclusive volatile' and 'shared volatile' while the specification fails to clearly redefine the terminology. The specification is filled with 'it may indicate' language (paragraph 0020 of the Applicant's specification for example although this language is used throughout the specification). If the language 'may indicate' a condition or state the implication is it 'may not indicate' such a condition or state as well. This is not a positive recitation of a meaning of the

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given terminology. The specification is written in such a way that not only the terminology is imprecise but the definitions or qualifications of the terminology is imprecise as well. This inhibits a clear understanding of the meaning of the actual language used in both the body of the specification and the claims which impacts a clear understanding of the claim language. It is true that the claims must be considered as a whole, however, this does not preclude there being problems with parts of the claims. The claims must be considered *as a whole in light of the specification*. In this present specification, the meaning of the cited terminology is ambiguous. The claim language uses the terms 'volatile' and 'non-volatile' in conjunction with cache lines and cache line segments without adequately providing meanings within the specification for this use of the terms. These terms are commonly associated with memory devices and not with data within a memory device or cache. This does not provide a clear, distinct description of the present invention within either the specification or in the claims themselves. The metes and bounds of the claim language cannot be determined.

15. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The terms "volatile" and "non-volatile" in the claims appear to be used by the claims to mean status conditions associated with data in a cache line or segments of a cache line, while the accepted meanings of these terms are descriptive of memory hardware devices and the loss of data when the memory device loses power. The terms are indefinite because the specification does not

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clearly redefine the terms. For instance, paragraphs 0021 and 0022 explain that there 'may' be no difference between a 'shared volatile state' and an 'exclusive volatile state' as both 'may include' segments of a cache in which segments are shared in either a volatile or non-volatile state. See MPEP 2111.01.

16. Due to the Applicant's insistence the following metes and bounds are given to the claim language and art has been applied using the an interpretation as given: 'modified segment' *may be* a segment that contains data that *may be* changed by the owning processor without notification to other processors or devices and a 'non-volatile segment' *may be* a segment that *may* generate a notification to a sharing processor or device if it is modified by the owning processor or device (e.g., see pages 8-9 of the appeal brief).

## *35 USC § 102*

17. The rejection of claims 1-9, 13-31, 34-36, 38-40 and 42-43 as being anticipated by Baylor et al. P/N 5,822,763 is ***withdrawn*** due to the amendment. The following rejection is given due to the amendment.

## *35 USC § 103*

18. The following is a quotation of 35 USC 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 1-9, 13-31, 34-36, 38-40 and 42-43 is rejected under 35 USC 103(a) as being unpatentable over Baylor et al. P/N 5,822,763.

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20. Baylor teaches the invention (claims 1, 9, 13, 17, 21, 26 and 29) as claimed including a device and method comprising:

means for storing data as being either caches or memory modules (e.g., see Figure 1);

means for tracking either a shared second state, a modified second state and an exclusive second state of cache line segments for the means for storing data as being a transient state of the data (e.g., see col. 2, line 61 to col. 3, line 2);

a first cache in a first central processing unit to store a first cache line in either a shared second state, an exclusive second state and a modified second state (e.g., see Figure 1, elements labeled by a 1);

a second cache in a second central processing unit in communication via a system interconnect with the first cache to store a second cache line (e.g., see Figure 1, elements labeled by a 2);

a first plurality of memory segments of a plurality of cache lines to track a second status for a subset of memory segments of the cache lines, wherein the second status requires that a modification to a segment of a cache line does not cause a notification of the modification to be sent, and wherein the second status comprises at least two statuses, a modified second status, a shared second status, or an exclusive second status for the second plurality of memory segments as cache lines being as state bits to global lines and global sub-lines (e.g., see col. 2, line 46-60);

wherein the modified second status identifies a cache line having a first status segment that is coherent between a plurality of caches associated with different processors and a second status segment that is not coherent between the plurality of caches as sub-lines of the caches having mixed states within a cache line (e.g., see col. 3, lines 25-34);

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wherein the shared second status identifies a cache line having a first status segment, a second status segment and a segment that is owned by a processor other than a processor associate with the cache and wherein the exclusive second status identifies a cache line having a first status segment that is shared between a plurality of caches associated with different processors and requires that a modification to a first status segment of a cache line cause a notification of the modification to be sent, and a second status segment that is shared between the plurality of caches as the processor caches share lines and sub-lines with the lines and sub-lines being in either a shared or exclusive state and in a modified state or valid or invalid state (e.g., see Figures 2-3);

circuitry to allow access to the plurality of memory segments as being inherent since the memory modules allow line and sub-line granularity (e.g., see col. 3, lines 25-34);

a pipeline to process instructions in either a program order or out of program order as a system capable of having a multi-stage interconnection network particularly as instructions must be processed or executed in either the program order or as out-of-order (e.g., see col. 2, lines 21-45);

a set of execution units to execute the instructions as multiple processors (e.g., see Figure 1);

a set of caches coupled to the pipeline to store data required by the pipeline in either a modified volatile, exclusive volatile or shared volatile state as private caches to the individual processors (e.g., see Figure 1);

filling a cache line by executing a first volatile load request as a processor read which does not change the state of the cache line and therefore does not require notification to other

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processors (e.g., see col. 5, lines 42-43);

receiving a first request for a first segment of the cache line and placing the requested data in a cache line as requesting sub-line sizes of data (e.g., see col. 2, lines 21-45);

indicating at least the first segment is in a first state that requires that a modification to a segment of a cache line cause a notification of the modification to be sent as that reading or writing to the first or any segment of a line requires a request to the global directory and permission must be granted from the global directory for the execution of the action requested (e.g., see col. 3, lines 3-16);

sending at least the first segment while maintaining a second segment of the cache line in s second state that requires that a modification to a segment of a cache line does not cause a notification of the modification to be sent as a sub-line being in a transient or non-transient state (e.g., see col. 3, lines 35-60); and,

placing an indication of a shared volatile state associated with the requested data in the cache line as signals or states placed in the global directory indicating the status of the requested data and the possible usage of the requested data (e.g., see col. 3, line 61 to col. 4, line 57).

Baylor teaches the elements related to the segments (sub-lines) within caches of a multiprocessor system. Coherency among a multiprocessor/cache system is detailed as given above, however, the limitations of notifications is not necessarily taught to the extent as claimed by the present claims. Baylor teaches maintaining coherency between caches which have the capability of using segments or sub-lines which can be updated or changed without invalidating the entire cache line. Coherency is maintained by the reference by using a global directory which stored the directory information of the sub-line entries. Notification is made by checking

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the global directory for access rights and data status prior to completing modification to data segments or sub-lines (e.g., see col. 2, line 22-60). It would have been obvious to one of ordinary skill in the cache art at the time the invention was made to equate the notification of segment or sub-line states and statuses to the coherency process of the Baylor reference because both are methods of maintaining data coherency in a multi-processing/multi-cache system for data segments smaller than a cache line size and notification is equivalent to passing information to all the processors in the system which has the data segment or sub-line in any state of modification, ownership or invalidation.

As to claim 2, Baylor teaches modifying a portion of the first segment of the cache line and sending a notification of the modification as the protocol necessary for accessing or modifying sub-lines of a cache line in the global directory (e.g., see Figure 3) with explanations of the state diagram given at (e.g., see col. 6, line 51 to col. 7, line 43).

As to claim 3, Baylor teaches modifying the second segment of the cache line without generating a notification of the modification and indicating the second segment is in a second state, wherein the second state comprises one of (a) a modified second state that identifies a cache line having a non-volatile segment that is coherent between a plurality of caches associated with different processors, and a second stat segment that is not coherent between the plurality of caches, and (b) an exclusive second state that identifies a cache line having a first state segment, a second state segment, and a segment that is owned by a processor other than a processor associate with the cache as the cache protocol including modifying any of the cache sub-lines as a processor accessing data in its associated cache with the data in the sub-line not being in a read-only status in its cache therefore a response from the directory is not required (e.g., see col.

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2, lines 46-60).

As to claim 4, Baylor teaches the cache line is a part of a first cache associated with a first processor (e.g., see Figure 1).

As to claim 5, Baylor teaches sending data from the cache line to a second cache associated with a second processor as sub-line data being transferred to the cache of a requesting processor (e.g., see col. 7, lines 6-27).

As to claim 6, Baylor teaches receiving a second request for a different third segment of the cache line and sending the third segment of the cache line while maintaining either the modified second state and exclusive second state as being able to process a request for any sub-line of a cache line when the data in the sub-line is modified (e.g., see col. 7, lines 6-27).

As to claim 7, Baylor teaches updating the cache line to indicate the third segment of the cache line is in a first state as updating the cache line segment or sub-line when the states of the cache line is transient therefore requiring permission from the global directory before the update is performed (e.g., see 3, lines 3-16).

As to claim 8, Baylor teaches updating the cache line such that only the third segment of the cache line is in a first state and invalidating the cache line from all other processors holding the cache line or sending an updated copy of the cache line to a processor as invalidating a cache line which is in a non-transient state (e.g., see col. 3, lines 17-34).

As to claim 14, Baylor teaches executing a load or a second state load request for data held in the cache line in a first state and returning the result of the second state load request as the data of any of the sub-lines of the cache line being in a shared or non-shared state and status bits for determining whether or not the global directory requires updating and granting of

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permission for a modification of any of the sub-lines of the cache line (e.g., see col. 3, lines 35-52).

As to 15, Baylor teaches executing a load or second volatile load request for a volatile portion of the cache line and placing the cache line in an invalid state being able to invalidate any sub-lines of a cache line (e.g., see col. 3, lines 35-52).

As to claim 16, Baylor teaches executing a load or second state load request for a second state portion of the cache line and receiving an updated copy of the cache line in a shared second state with requested data in a first state as being shown in the state diagram for any of the sub-lines of a cache line (e.g., see Figure 3).

As to claim 18, Baylor teaches a means for indicating a first portion and a second portion of a segment of the means for storing data contains first state data, wherein a first state requires that a modification to a segment of a cache line cause a notification to the modification to be sent as status data for sub-lines of a cache line which require permission from the global directory for modifying any of the sub-lines (e.g., see col. 2, line 61 to col. 3, line 16).

As to claim 19, Baylor teaches a means for notifying a second means for storing data that a first state data has been modified, wherein a first state requires that a modification to a segment of a cache line cause a notification of the modification to be sent as handshaking (e.g., see col. 2, line 61 to col. 3, line 2).

As to claim 20, Baylor teaches a means for indicating multiple segments are in either a volatile or non-volatile state for a line of the means for storing data as maintaining status at a sub-line granularity level (e.g., see Figure 3 with the description of this figure in col. 3, line 51 to col. 4, line 43).

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As to claim 22, Baylor teaches a first processor associated with the first cache and a second processor associated with the second cache (e.g., see Figure 1).

As to claim 23, Baylor teaches a system memory that is cached by the first and second caches (e.g., see col. 1, lines 29-42).

As to claim 24, Baylor teaches the first cache line indicates at least one non-volatile segment as the global directory containing status for both a global line and global sub-line for each line and sub-line entry (e.g., see col. 2, lines 46-60).

As to claim 25, Baylor teaches the first cache notifies the second cache of a change in the non-volatile portion of a cache line in either a modified volatile state, an exclusive volatile state or a shared volatile state as sub-line data being transferred to the cache of a requesting processor (e.g., see col. 7, lines 6-27).

As to claims 27 and 30, Baylor teaches the cache generates a notification upon modification of non-volatile data as responses from the global directory for updating both the data and the status bits of either/or the cache line or sub-lines (e.g., see col. 2, line 61 to col. 3, line 16).

As to claim 28, Baylor teaches the cache shares data containing a modified portion as a line mixed state where at least two caches have the same data but not every copy of the data is still valid indicating a sub-line of the cache line has been modified by one of the processors (e.g., see col. 3,lines 25-34).

As to claim 31, Baylor teaches indicating the size and position of a non-volatile portion of a cache line as sub-line granularity of the coherence protocol (e.g., see 2, lines 23-60).

As to claim 34, Baylor teaches the present invention wherein the notification is sent to a

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processor that: does not own the modified segment, holds the modified segment in a cache line of a cache associated with the notified processor, or does not hold the modified segment in a cache line of a cache associated with the notified processor (e.g., see col. 7, lines 6-40).

As to claim 35, Baylor teaches the present invention wherein the cache line further comprises a lock field, a data field and a status field, the status field to indicate a volatile status comprising one of a modified volatile state, a shared volatile state and an exclusive volatile state as the cache being in either a lockup state or a lockup free state indicating only the processor having ownership can process requests to the cache line or cache sub-line, the cache lines and sub-lines also contains data as well as status bits (e.g., see Figure 2 and col. 4, line 58 to col. 5, line 7).

As to claim 36, Baylor teaches the present invention wherein the cache line further comprises a second segment in a volatile state and a third segment in a non-volatile state as the sub-lines within the cache line can be in different ownership states and different coherency states (e.g., see col. 7, lines 6-40).

As to claim 38, Baylor teaches the present invention wherein a modified volatile state identifies a cache line having a non-volatile segment that is coherent between a plurality of caches associated with different processors and a volatile segment that is not coherent between the plurality of caches; an exclusive volatile state identifies a cache line having a non-volatile segment, a volatile segment and a segment that is owned by a processor other than a processor associated with the cache; and a shared volatile state identifies a cache line have a non-volatile segment that is shared between a plurality of caches associated with different processors and a volatile segment that is shared between the plurality of caches as maintaining coherency of the

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sub-lines dependent upon ownership of sub-lines or segments of cache lines and when a owner processor modifies a sub-line of the cache or a processor without ownership modifies a sub-line of the cache (e.g., see col. 7, lines 6-40).

As to claim 39, Baylor teaches the present invention wherein the cache line further comprises a lock field, a data field and a status field, the status field to indicate a volatile status comprising one of a modified volatile state, a shared volatile state and an exclusive volatile state as the cache being in either a lockup state or a lockup free state indicating only the processor having ownership can process requests to the cache line or cache sub-line, the cache lines and sub-lines also contains data as well as status bits (e.g., see Figure 2 and col. 4, line 58 to col. 5, line 7).

As to claim 40, Baylor teaches the present invention wherein the segment is a first segment; and wherein the cache line further comprises a second segment in a volatile state and a third segment in a non-volatile state, a non-volatile state requires that a modification to a segment of a cache line cause a notification of the modification to be sent and a volatile state requires that a modification to a segment of a cache line does not cause a notification of the modification to be sent as maintaining coherency of the sub-lines dependent upon ownership of sub-lines or segments of cache lines and when a owner processor modifies a sub-line of the cache or a processor without ownership modifies a sub-line of the cache (e.g., see col. 7, lines 6-40).

As to claim 42, Baylor teaches the present invention further comprising means for tracking a lock field and a data field for the means for storing data as the cache being in either a lockup state or a lockup free state indicating only the processor having ownership can process

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requests to the cache line or cache sub-line, the cache lines and sub-lines also contains data as well as status bits (e.g., see Figure 2 and col. 4, line 58 to col. 5, line 7).

As to claim 43, Baylor teaches the present invention further comprising means for tracking a volatile state and a non-volatile state for the means for storing data, a non-volatile state requires that a modification to a segment of a cache line cause a notification of the modification to be sent and a volatile state requires that a modification to a segment to a cache line does not cause a notification of the modification to be sent as maintaining coherency of the sub-lines dependent upon ownership of sub-lines or segments of cache lines and when a owner processor modifies a sub-line of the cache or a processor without ownership modifies a sub-line of the cache (e.g., see col. 7, lines 6-40).

## *RESPONSE TO APPLICANT'S REMARKS*

21. Applicant's arguments filed June 24, 2008 have been fully considered but they are not persuasive.

22. As to the Applicant's removing the terms 'volatile' and 'nonvolatile' from most of the claims, the states and statuses of the application must still rely on this terminology as support from the specification since it is the basis of the states and statuses described. The rejections previously given are still valid.

23. The Applicant is continuing to use and defend the terms 'volatile' and 'nonvolatile' in the disclosure and the claims. Applicant is using these terms in conjunction with known terms in the art which describe cache coherency for lines and line segments. Terms for ownership of cache data and the state of cache data with other memory devices within a system are already known, however, when combined with the terms 'volatile' and 'nonvolatile' the meaning of the ownership

and coherency terminology becomes confusing and ambiguous.

24. The terminology does not have to be associated with a different art for there meaning to be set in the memory arts. The reasons are repeated from the previous office actions and shown below. A person of ordinary skill in the memory art will not necessarily understand volatile and nonvolatile states when combined with modified and exclusive states of cache segments.

25. The Applicant is essentially presenting a defense of the use of the terms 'volatile' and 'nonvolatile' as being valid because these terms are being used based upon a normal (non-memory art specific definition) dictionary meaning but also that these terms are not ambiguous because they are well known in the memory art. The definitions of these terms in the memory art are very specific and while the technical definitions used by one of ordinary skill in the memory arts is not basically contrary to the standard dictionary definitions, the technical definitions go beyond the dictionary definitions in such a way that the Applicant's use of these terms is confusing and renders the claims indefinite. Such well known, established technical usage of terms cannot be used without specific, consistent redefinition of the terms by the Applicant. The terms 'volatile' and 'non-volatile' are used in the memory arts to describe memory storage devices. These terms have a long established definition which is tied to the actual hardware used for memory. Using these terms in the context of describing 'states' of cache lines is outside of the given practices.

26. The dictionary definitions provided by the Applicant to support the use of the terms 'volatile' and 'non-volatile' in the present specification further confuse the use of these terms instead of clarifying their usage. The meanings found in investment dictionaries and medical dictionaries are not pertinent to usage of these terms in relationship to computer memory.

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Computer memory is the field of use for the present invention and there is no application in the fields of chemistry, finance or medicine. The one definition provided in the computer arts is for programming variables. The claims as well as the specification is directed toward cache lines and replacement protocol. This is not the same usage as programming variables. No where in the Applicant's specification is there a discussion of either programming variables, static variables, volatile variables or non-volatile variables.

27. Applicant's representative refers to the examiner's use of 'undue experimentation' as being the basis of the lack of enablement rejection, however, this was never used in the previous rejections. The objection and rejection has always been directed to misuse of terms in the art which already have established definitions in the memory art. By focusing on explanations as to why 'undue experimentation' is inappropriate, the prosecution of the given claims is being confused and obscured. The factors discussed on page 6 of the Appeal Brief filed March 26, 2207, relate specifically to the use of 'undue experimentation' for an enablement requirement rejection. 'Undue experimentation' was not the basis of the rejection for failing to comply with the enablement requirement.

28. As to the Baylor reference not teaching states in relationship to segments of cache lines, this exact concept is stated in col. 2, lines 36-45. Sub-lines are maintained with both residence and modified bits which indicates the ownership of a sub-line or segment and whether or not the sub-line or segment is coherent with the other memories in the system.

## *OFFICE ACTION FINALITY*

29. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

## *CONCLUSION*

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

/Reba I. Elmore/
Primary Patent Examiner
Art Unit 2189

Tuesday, September 09, 2008

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